WHAT IS CLAIMED IS:

1. An equalizing circuit comprising:

a memory control unit which receives an input of an input image data signal;

a register setting unit which receives setting of a main scan coordinate and a subscan coordinate to start at least the equalizing of the input image data signal;

an equalizing control unit which starts the equalizing of the input image data signal from the main scan coordinate and the subscan coordinate, which are set by the register setting unit, and outputs the equalized image data signal; and

an output control unit which receives an input of an equalized image data signal from the equalizing control unit and outputs it as an output image data signal.

2. An equalizing circuit according to claim 1,

wherein the register setting unit receives setting with respect to a size of an equalized block as an unit for equalizing the input image data.

3. An equalizing circuit according to claim 1,

wherein the register setting unit receives setting of a skew value of an equalized block as an unit for equalizing the input image data.

4. An equalizing circuit according to claim 1,

wherein the equalizing control unit performs a

predetermined process outside of an output image region at least at an upper end, a lower end, a right end and a left end of the input image data signal.

5. An equalizing circuit according to claim 1, wherein the memory control unit delays the input image data signal by lines and controls the delayed input image data signal so that it is output to the equalizing control unit.

6. An equalizing circuit according to claim 1, wherein the equalizing control unit further has an equalized matrix generating/calculating circuit which is used in common independently of a size of the equalized block.

7. An equalizing circuit according to claim 1, wherein the equalizing control unit performs a predetermined delay adjustment in such a manner that it performs the equalizing at a certain timing independently of a skew value of the equalized block.

8. An image processing circuit comprising:

a memory control unit which receives an input of an input image data signal;

a first memory which stores the input image data signal after delaying it;

a CPU which designates at least any one of a main scan coordinate and a subscan coordinate to start equalizing of the input image data signal, a main scan size and a subscan size of the equalized block and skew

values in a main scan direction and in a subscan direction of the equalized block;

a register setting unit which holds the setting information which is designated by the CPU;

an equalizing control unit which performs the equalizing of the input image data signal at a certain timing independently of a skew value of the equalized block on the basis of the setting information held by the register setting unit and outputs the equalized image data signal;

a second memory which receives an input of the equalized image data signal from the equalizing control unit and holds it as an output image data signal; and

an output control unit which outputs the output image data of the second memory.

9. An image processing circuit according to claim 8,

wherein the equalizing control unit further has an equalized matrix generating/calculating circuit which is used in common independently of a size of the equalized block.

10. An equalizing circuit comprising:

memory control means for receiving an input of an input image data signal;

register setting means for receiving setting of a main scan coordinate and a subscan coordinate to start at least the equalizing of the input image data signal;

equalizing control means for starting the equalizing of the input image data signal from the main scan coordinate and the subscan coordinate, which are set by the register setting unit, and outputting the equalized image data signal; and

output control means for receiving an input of an equalized image data signal from the equalizing control unit and outputting it as an output image data signal.

11. An image processing circuit comprising:

memory control means for receiving an input of an input image data signal;

first storing means for storing the input image data signal after delaying it;

control means for designating at least any one of a main scan coordinate and a subscan coordinate to start equalizing of the input image data signal, a main scan size and a subscan size of the equalized block and skew values in a main scan direction and in a subscan direction of the equalized block;

register setting means for holding the setting information which is designated by the control means;

equalizing control means for performing the equalizing of the input image data signal at a certain timing independently of a skew value of the equalized block on the basis of the setting information held by the register setting unit and outputting the equalized image data signal;

second storing means for receiving an input of the equalized image data signal from the equalizing control unit and holding it as an output image data signal; and

output control means for outputting the output image data of the second storing means.

12. An equalizing method comprising:

receiving an input of an input image data signal from a memory control unit;

receiving setting of a main scan coordinate and a subscan coordinate to start at least the equalizing of the input image data signal by a register setting unit;

starting the equalizing of the input image data signal from the main scan coordinate and the subscan coordinate, which are set by the register setting unit, and outputting the equalized image data signal by an equalizing control unit; and

receiving an input of the equalized image data signal and outputting it as an output image data signal by an output control unit.

13. An equalizing method according to claim 12,

wherein, when the register setting unit receives setting with respect to a size of an equalized block as an unit for equalizing the input image data, the equalizing control unit performs the equalizing on the basis of the present equalized block.

14. An equalizing method according to claim 12,

wherein the register setting unit receives setting

of a skew value of an equalized block as an unit for equalizing the input image data.

15. An equalizing method according to claim 12, wherein the equalizing control unit performs a predetermined process outside of an output image region at least at an upper end, a lower end, a right end and a left end of the input image data signal.

16. An equalizing method according to claim 12, wherein the memory control unit delays the input image data signal by lines and controls the delayed input image data signal so that it is output to the equalizing control unit.

17. An equalizing method according to claim 12, the equalizing control unit sets an equalized block as an unit of the equalizing by a certain mode signal.

18. An equalizing method according to claim 12, wherein the equalizing control unit performs a predetermined delay adjustment in such a manner that it performs the equalizing at a certain timing independently of a skew value of the equalized block.

19. An image processing method comprising:

receiving an input of an input image data signal by a memory control unit;

storing the input image data signal after delaying it by a first memory;

designating at least any one of a main scan

coordinate and a subscan coordinate to start equalizing of the input image data signal, a main scan size and a subscan size of the equalized block and skew values in a main scan direction and in a subscan direction of the equalized block by a CPU;

holding the setting information which is designated by the CPU at a register setting unit;

performing the equalizing of the input image data signal at a certain timing independently of a skew value of the equalized block on the basis of the setting information held by the register setting unit and outputting the equalized image data signal by an equalizing control unit;

receiving an input of the equalized image data signal from the equalizing control unit and holding it as an output image data signal by a second memory; and

outputting the output image data of the second memory by an output control unit.